* Sequential logic Circuits :-

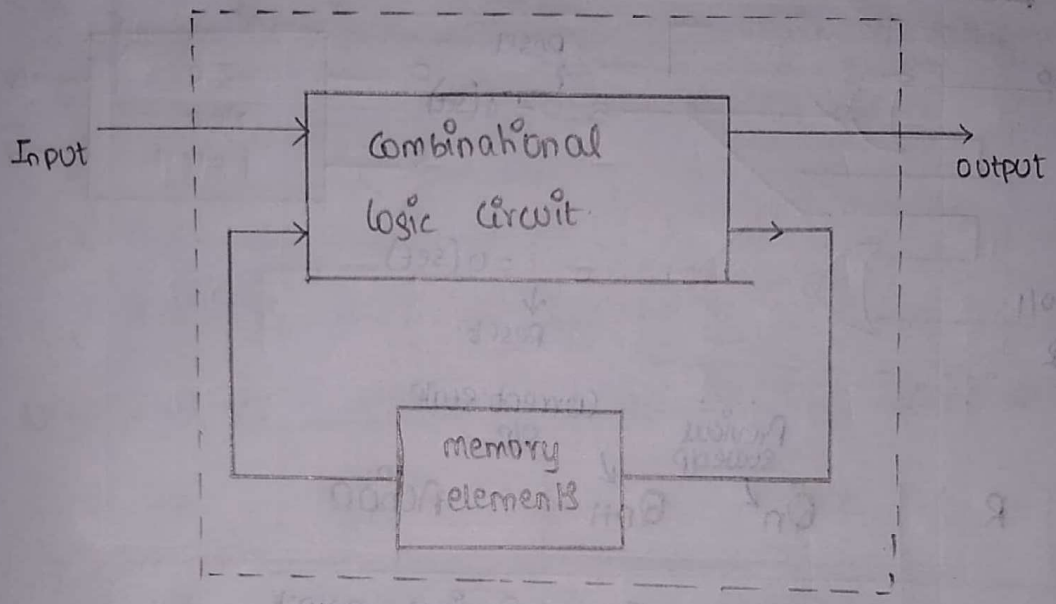
Latch , Flip Flop , Types of Flip-Flops

Types of Flip Flops

- SR Flip Flop
- D Flip Flop
- JK Flip Flop
- T Flip Flop

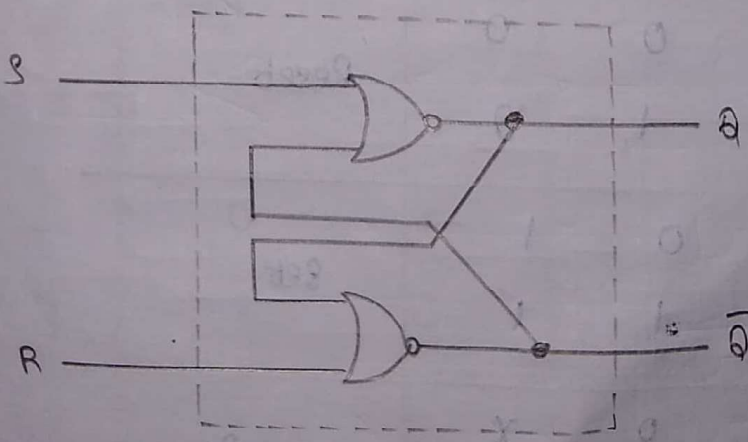
Latch

- NOR Latch
- NAND Latch



Block Diagram of Sequential logic Circuit

* NOR Latch :- (SR LATCH)

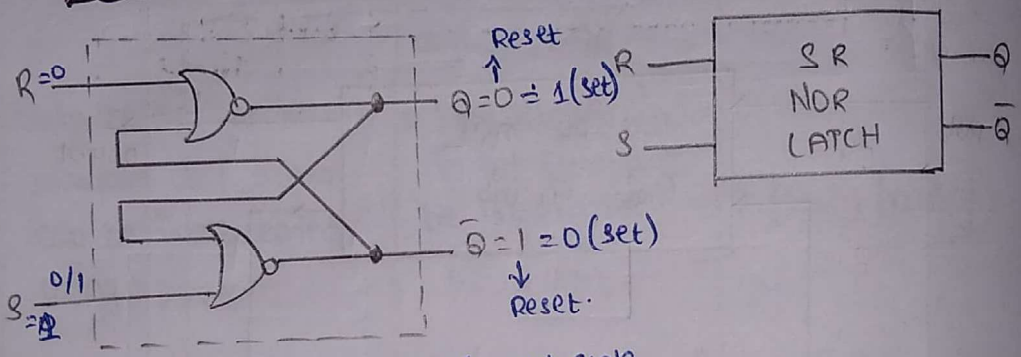


* TRUTH TABLE

S	R	Q	$\bar{Q}$	Action
0	0	Q	$\bar{Q}$	No change
0	1	0	1	Reset
1	0	1	0	set
1	1	X	X	Invalid

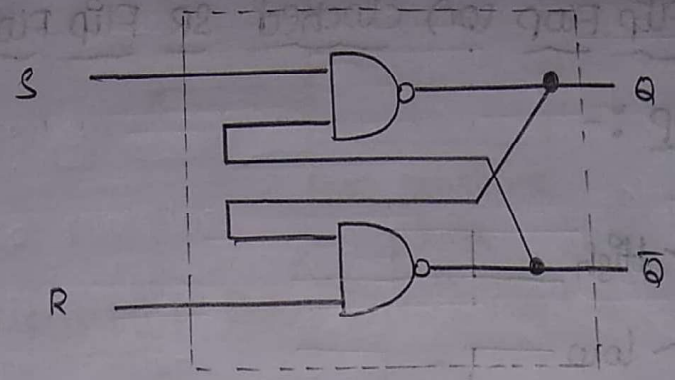
A	B	Nor
0	0	1
0	1	0
1	0	0
1	1	0

* Active high SR LATCH :- (NOR LATCH)



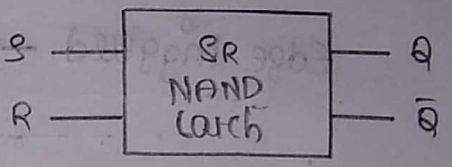
S	R	Previous state o/p Q_n	Current state o/p Q_{n+1}	Action
0	0	0	0	Previous output (or) No change
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	set
1	0	1	1	
1	1	0	X	Invalid.
1	1	1	X	

* Active low SR LATCH :- (NAND LATCH)



A	B	NAND
0	0	1
0	1	1
1	0	1
1	1	0

S	R	Q	$\bar{Q}$	Action
0	0	X	X	Invalid or Indt
0	1	1	0	Set
1	0	0	1	Reset
1	1	Q	$\bar{Q}$	No change

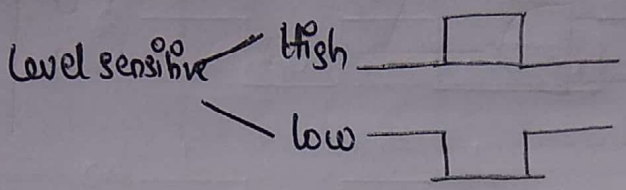


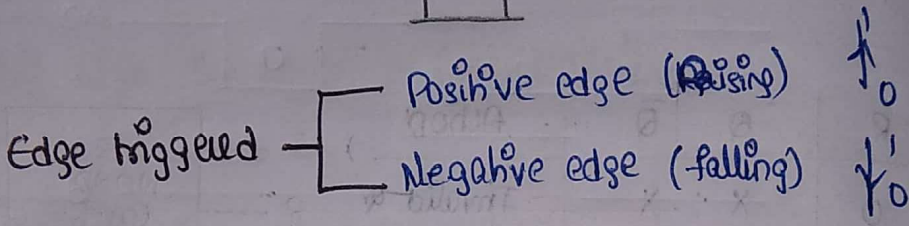
NOTE:- Invalid Conditions are called as Race around conditions.

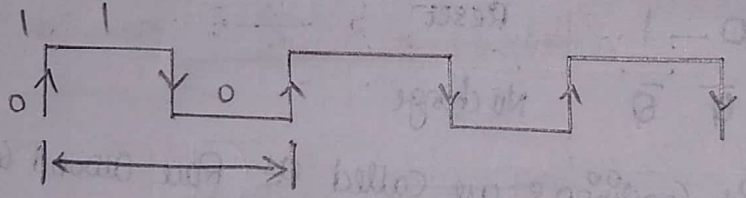
S	R	Q_n	Q_{n+1}	Action
0	0	0	X	In-valid (or) indeterminant
0	0	1	X	
0	1	0	1	Set
0	1	1	1	
1	0	0	0	Reset
1	0	1	0	
1	1	0	0	Previous o/p (or) No change
1	1	1	1	

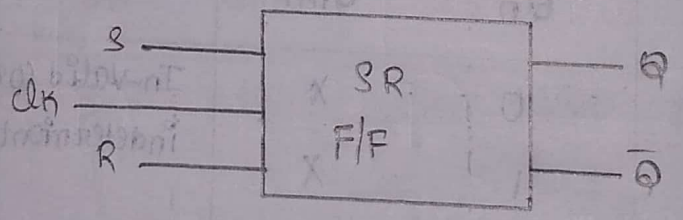
* Flip Flops:-

→ Gate SR Flip Flop (or) clocked SR Flip Flop (or) SR Flip Flop :-

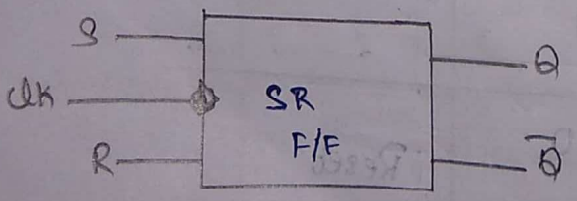




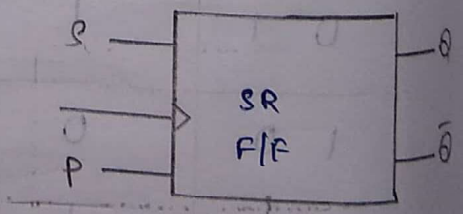




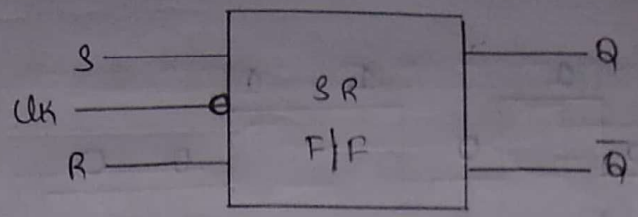
High sensitive Clock



Negative Edge clock

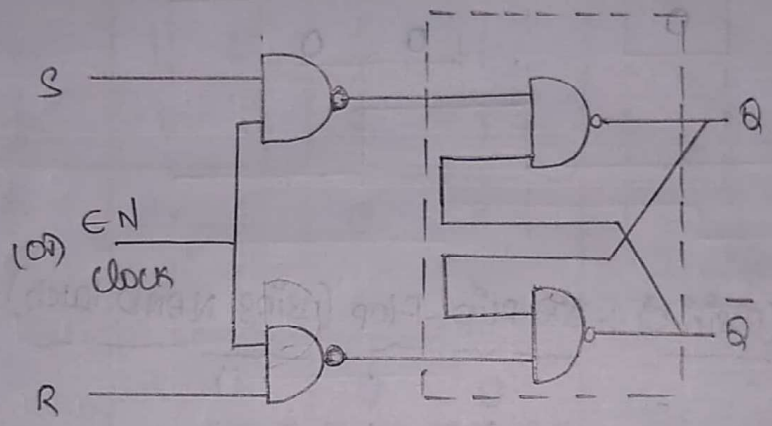


positive Edge clock



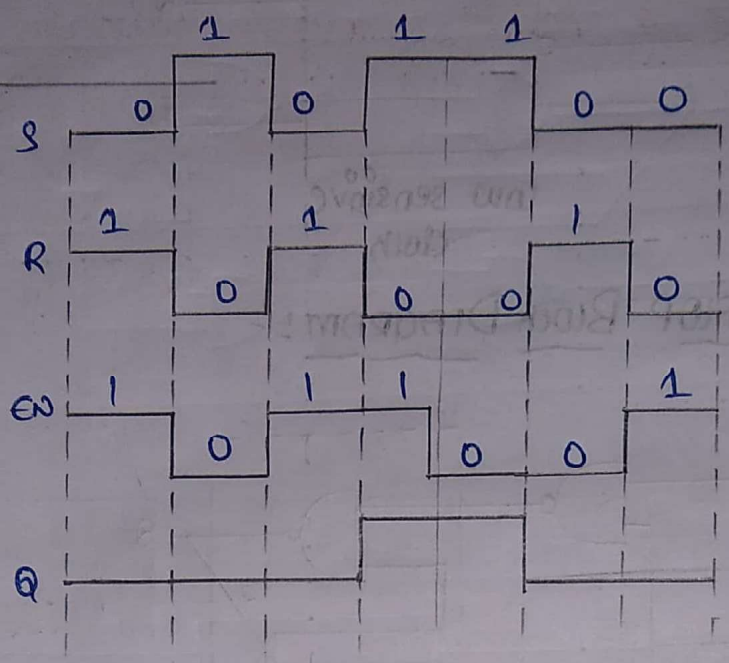
Low sensitive clock

* SR FLIPFLOP Block DIAGRAM :-

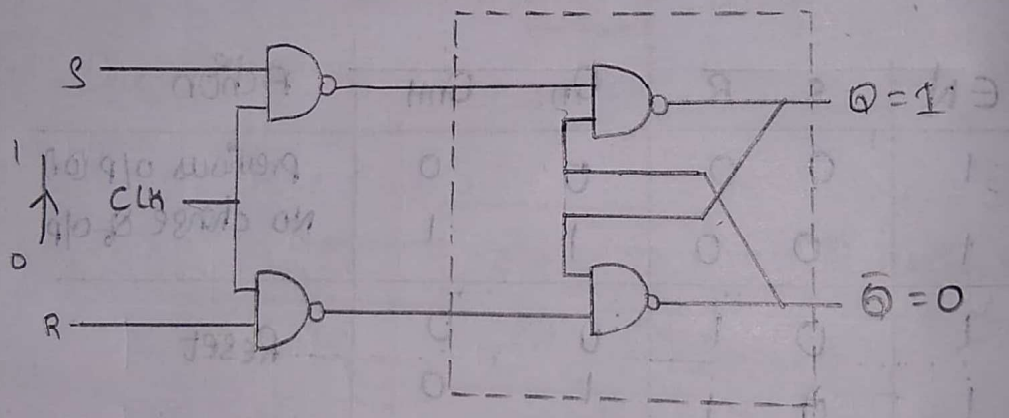


EN	S	R	Q_n	Q_{n+1}	Action
1	0	0	0	0	previous o/p (Q)
1	0	0	1	1	No change in o/p
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set
1	1	0	1	1	
1	1	1	0	X	Invalid.
1	1	1	1	X	
0	X	X	0	0	No change
0	X	X	1	1	

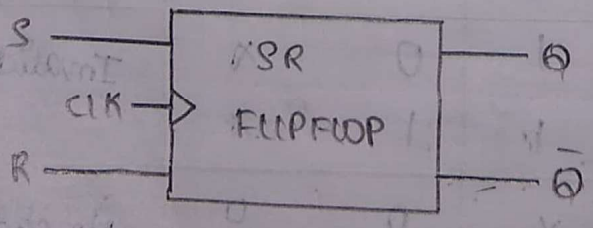
* Timing Diagram:-



* Edge triggered (Positive) :- SR Flip-Flop (using NAND latch):-



SR NAND LATCH

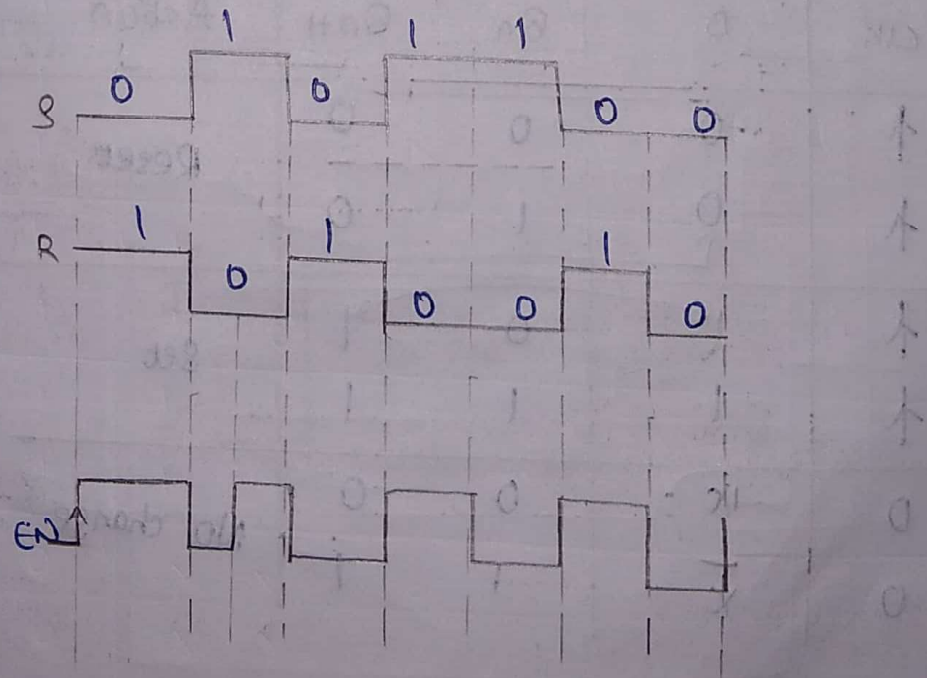


BLOCK DIAGRAM

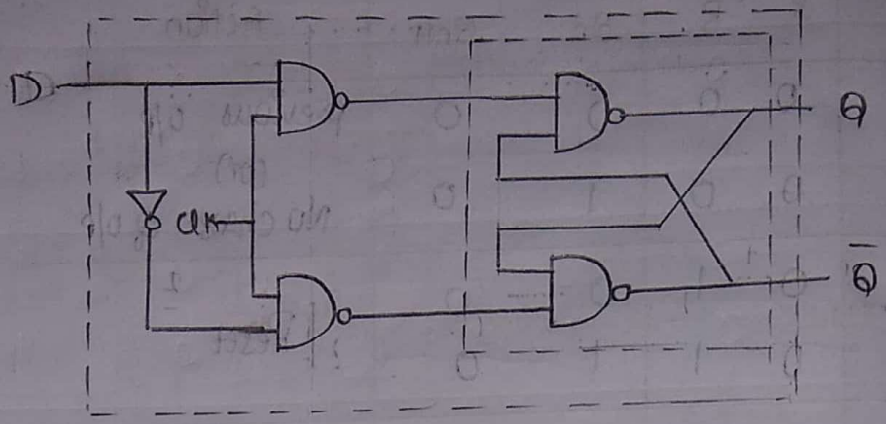
* SR F/F Truth table:-

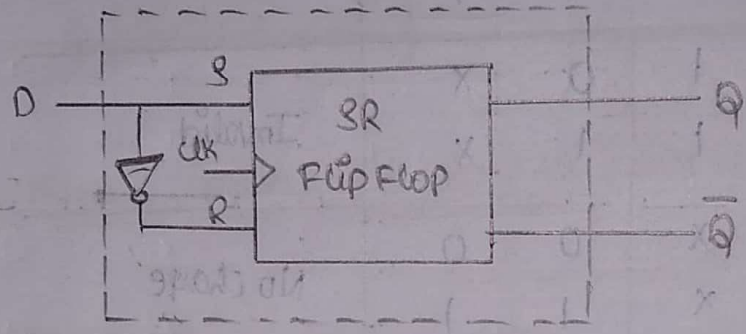
CLK	S	R	Q_n	Q_{n+1}	Action
↑	0	0	0	0	Previous o/p (or) No change of o/p
↑	0	0	1	0	
↑	0	1	0	0	Reset
↑	0	1	1	0	
↑	1	0	0	1	Set
↑	1	0	1	1	
↑	1	1	0	x	Invalid
↑	1	1	1	x	
0	x	x	0	0	No change
0	x	x	1	1	

* Timing diagram:-



* Positive Edge triggered D Flip Flop:-

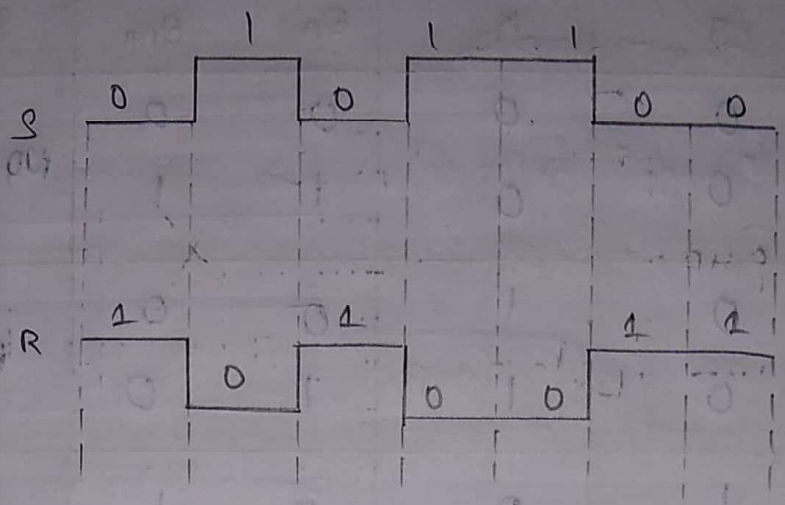




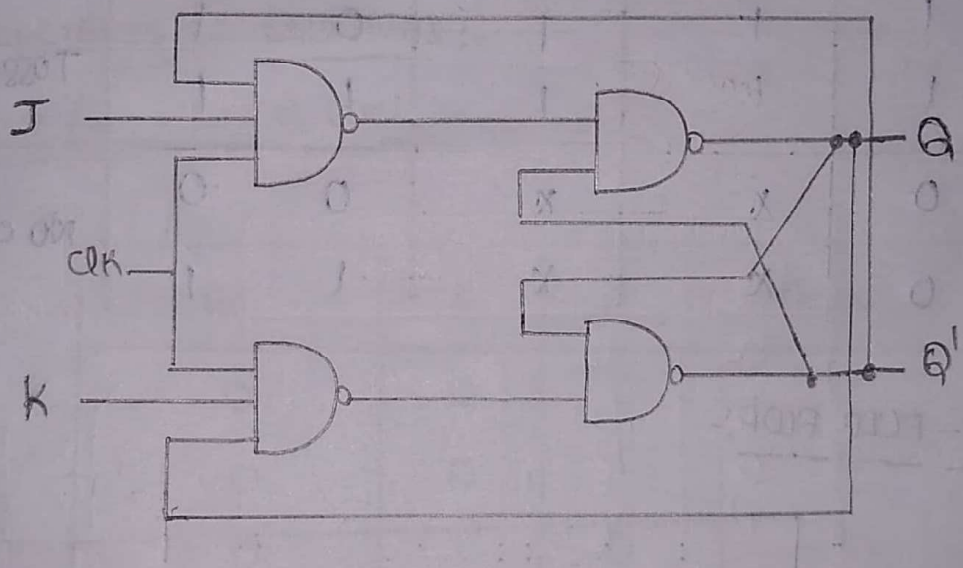
* D F/F Truth table:-

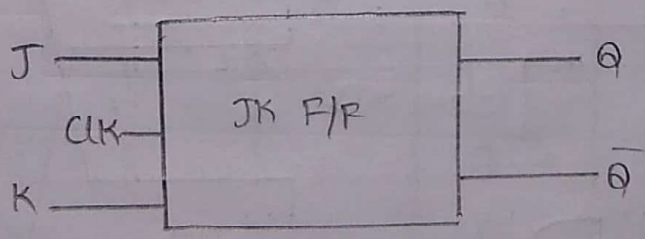
clk	D	Q_n	Q_{n+1}	Action
↑	0	0	0	Reset
↑	0	1	0	
↑	1	0	1	Set
↑	1	1	1	
0	x	0	0	No change
0	x	1	1	

* Timing Diagram:-



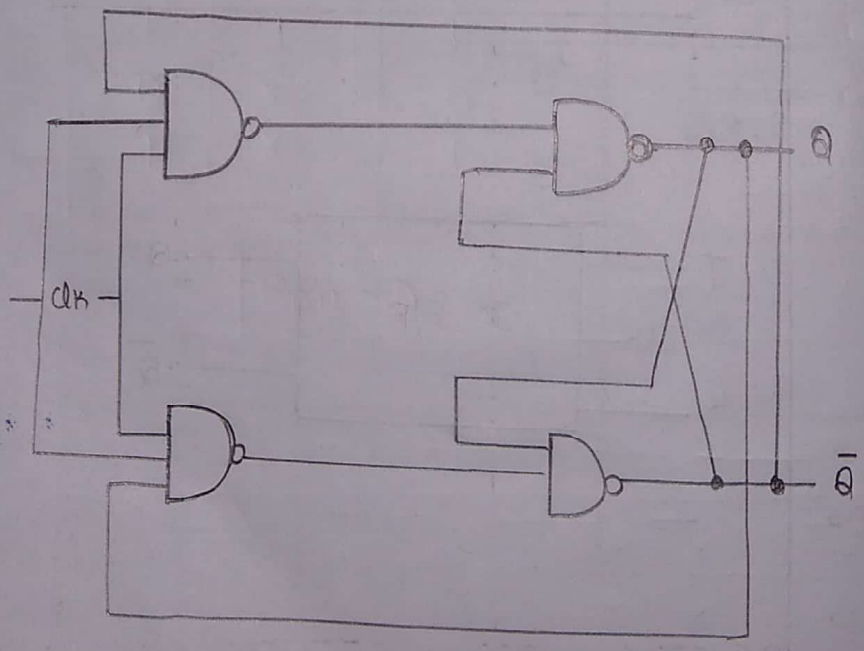
* JK FLIP FLOP:-





CLK	J	K	Q_n	Q_{n+1}	State
1	0	0	0	0	No change
1	0	0	1	1	
1	0	1	0	0	Reset
1	0	1	1	0	
1	1	0	0	1	Set
1	1	0	1	1	
1	1	1	0	1	Toggle
1	1	1	1	1	
0	x	x	0	0	No change
0	x	x	1	1	

* T- FLIP FLOP:-



Clk	T	Present state Qn	Next state Qn+1	State
1	0	0	0	No change
1	0	1	1	
1	1	0	1	Toggle
1	1	1	0	
0	x	0	0	No change
0	x	1	1	

* CHARACTERISTIC EQUATIONS :-

S-R (Set - Reset) Latch :-

Qn	S	R	Qn+1	
0	0	0	0	0
0	0	1	0	1
0	1	0	1	2
0	1	1	(x) Invalid	3
1	0	0	1	4
1	0	1	0	5
1	1	0	1	6
1	1	1	Invalid (x)	7

* Characteristic equation:-

$$Q_{n+1} = S + R'Q_n$$

$\Rightarrow (Q_n + \bar{Q}_n)(SR + S\bar{R}) + Q_n(\bar{S}\bar{R} + S\bar{R})$

$\Rightarrow (1)\ S(R + \bar{R}) + Q_n\bar{R}(\bar{S})$

$Q_{n+1} = S + \bar{R}Q_n$ (or) $S + R'Q = Q_{n+1}$

Q_n \	$S\bar{R}$	$\bar{S}\bar{R}$	SR	$S\bar{R}$
$\bar{Q}_n$	0 (0)	0 (1)	X (3)	1 (2)
Q_n	1 (4)	0 (5)	X (7)	1 (6)

$$Q_{n+1} = S + \bar{R}Q_n$$
$$= 1 + (\bar{0} \cdot 1)$$
$$= 1 + 1 = 1$$

* D F/F $\rightarrow Q_{n+1}$

Q_n	D	Q_{n+1}	
0	0	0	0
1	0	0	1
0	1	1	2
1	1	1	3
0	X	0	
1	X	1	

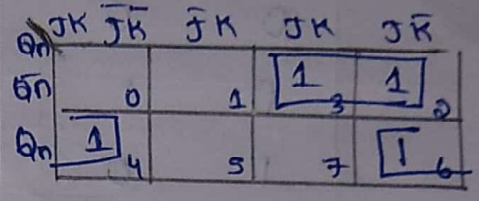
$Q_{n+1} = D$

Q_n \	D	$\bar{D}$
$\bar{Q}_n$	0 (0)	1 (1)
Q_n	0 (2)	1 (3)

$D(Q_n + \bar{Q}_n)$
$= D$

* JK FlipFlop

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

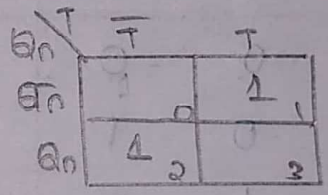


$Q_{n+1} = \bar{Q}_n (JK + J\bar{K}) + Q_n (\bar{J}\bar{K} + J\bar{K})$

$$Q_{n+1} = \bar{Q}_n J + \bar{K} Q_n$$

* T Flip Flop:-

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0



$$Q_{n+1} = \bar{T} Q_n + T \bar{Q}_n$$

* Excitation table for all flipflop.

* SR FlipFlop:-

Present Q_n	Next Q_{n+1}	Required i/p's S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

* D Flip Flop:-

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

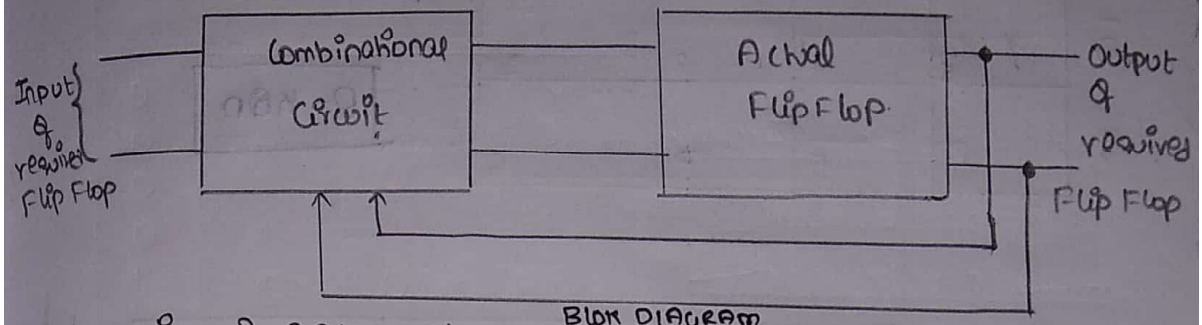
* JK Flip Flop:-

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

* T Flip Flop

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

* Conversion of one Flip Flop to another Flip Flop



BLOCK DIAGRAM

* Conversion of SR to JK F/F :-

Excitation table

Required F/F Input J	K	Present state Q_n	Next state Q_{n+1}	Actual F/F i/p's S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

J K Truth table

* Excitation table

Q_n	Q_{n+1}	S R
0	0	0 X
0	1	1 0
1	0	0 1
1	1	X 0

T/T → Required F/F

Extention table → Actual F/F

$S(JK, Q_n) = ?(J\bar{Q}_n$

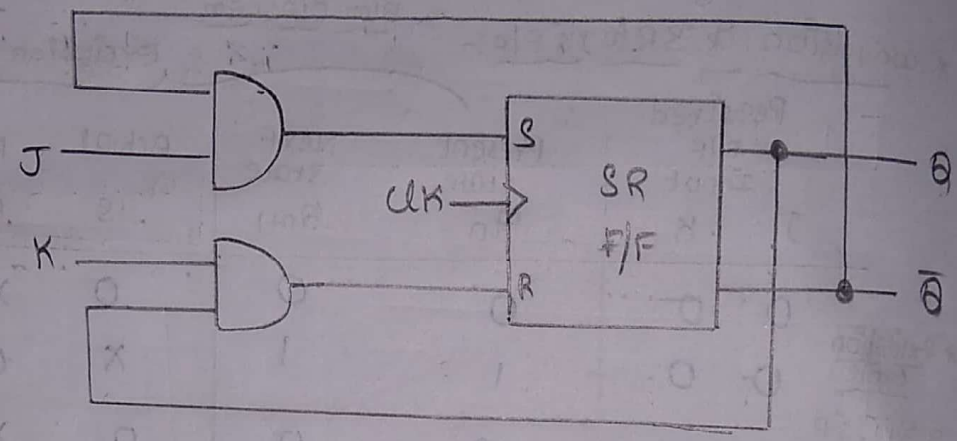
$\bar{Q}_n$ \	$Q\bar{K}$	$\bar{Q}\bar{K}$	QK	$\bar{Q}K$
Q	6	X 1	3	2
J	1 4	X 5	7	1 6

$S = J(\bar{Q}_n \bar{K} + \bar{Q}_n \bar{K})$

$\boxed{S = J\bar{Q}_n}$

$\bar{J}$ / J	$K\bar{Q}_n$	$\bar{K}\bar{Q}_n$	$K Q_n$	$K\bar{Q}_n$
$\bar{J}$	X 0	1	3	2
J	4	5	7	6

$R = KQ_n$



* Conversion of JK F/F to SR F/F :-

* Excitation :

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

S	R	Q_n	Q_{n+1}	J	K
0	0	0	0	0	X
0	0	1	1	X	0
0	0	0	0	0	X
0	1	1	0	X	1
1	0	0	1	1	X
1	0	1	1	X	0
1	1	0	X	1	X
1	1	1	X	X	1

$J(S, R, Q_n) = ?$

$\bar{S}$ / S	$\bar{R}\bar{Q}_n$	$\bar{R}Q_n$	RQ_n	$R\bar{Q}_n$
$\bar{S}$	0	X 1	X 3	2
S	1 4	X 5	X 7	1 6

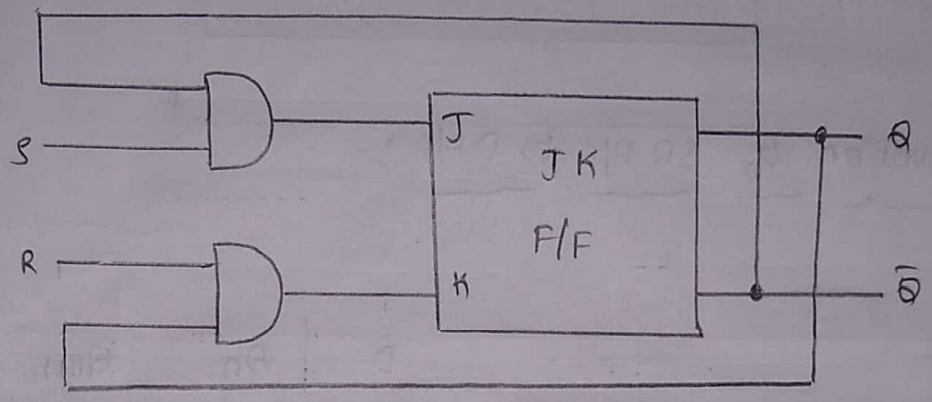
$J = S(\bar{R}\bar{Q}_n + R\bar{Q}_n)$

$J = S\bar{Q}_n$

$K = (J, R, Q_n) = ?$

	$\bar{R}\bar{Q}_n$	$\bar{R}Q_n$	RQ_n	$R\bar{Q}_n$
$\bar{S}$	X 0	1	1 3	X 2
S	X 4	5	1 7	X 6

$K = RQ_n$



* Convert D F/F to SR F/F :-

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

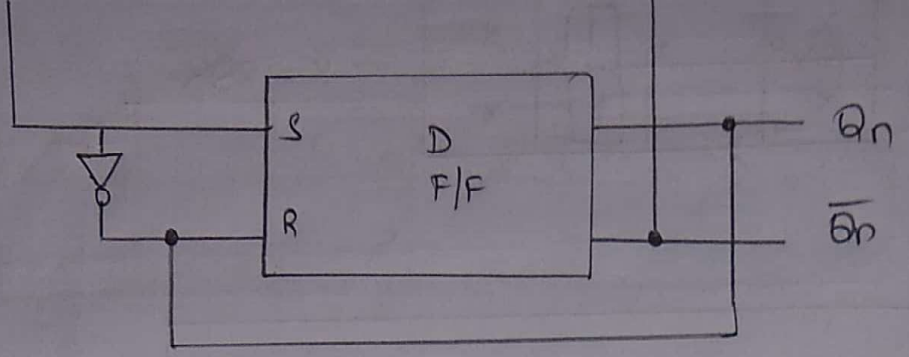
S	R	Q_n	Q_{n+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

$D = (S, R, Q_n) =$

	$\bar{R}\bar{Q}_n$	$\bar{R}Q_n$	RQ_n	$R\bar{Q}_n$
$\bar{S}$	0	1 1	3	2
S	1 4	1 5	7	1 6

$\Rightarrow \bar{R}Q_n(\bar{S}+S) + S(\bar{R}\bar{Q_n} + RQ_n)$

$\Rightarrow RQ_n + S\bar{Q_n}$



* Convertion of SR F/F to D F/F :-

Qn	Qn+1	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

D	Qn	Qn+1	S	R
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0

$S(D, Qn) = \overline{D}$

D \ $\overline{Qn}$ Qn	$\overline{Qn}$	Qn
$\overline{D}$	0	1
D	1 (2)	1 3

$\Rightarrow D(\overline{Qn} + Qn)$

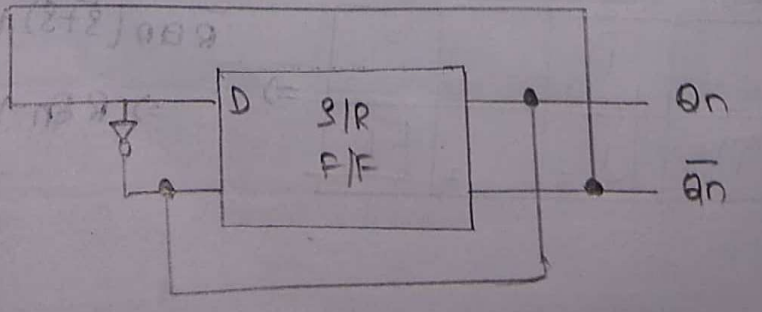
$= D$

$R(D, Qn)$

$\overline{D}$ \ $\overline{Qn}$ Qn	$\overline{Qn}$	Qn
$\overline{D}$	1 0	1
Qn	2	3

$\Rightarrow \overline{D}(\overline{Qn} + Qn)$

$= \overline{D}$



UNIT-5

SEQUENTIAL LOGIC CIRCUITS - II

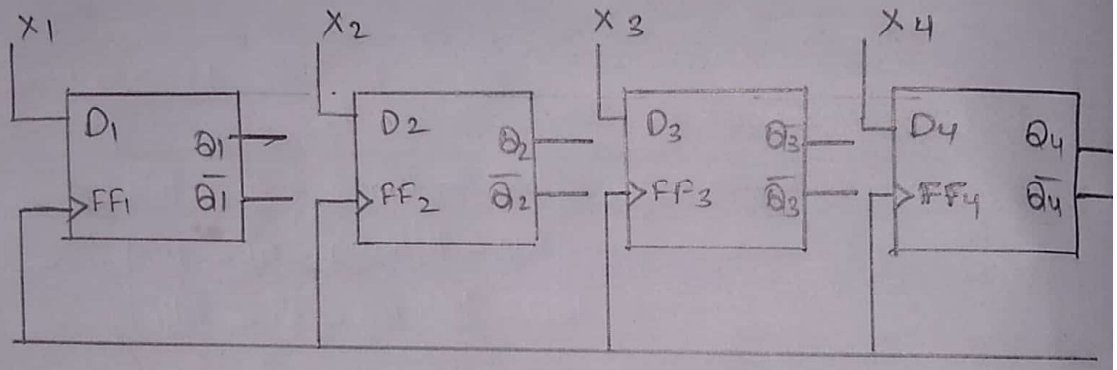
State machines

(Registers & Counters)

* **Registers:-**

→ shift registers

→ Buffer Registers (Parallel input (or) output) :-



→ Controlled buffer Register :-